APPENDIX A

CLAIMS AS AMENDED WITHOUT UNDERLINES OR BRACKETS

Please amend claims 42, 43, 45, 46, 48, 49, 57, 58, 61, 63, 70, 89, 90, 92, 94 - 97, 100 - 102, 105, 107, 108, 110, 112, 114, 116, 118, 120, 122, 124, 132, 140, 142, 144, 146, 148, 156 - 159, 166, 168, 184, 202, and 220, as follows:

42. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

storing digital signal processor operands in an integrated circuit alterable memory;

generating input information;

generating signal processed information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the signal processed information.

43. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;

generating signal processed information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the signal processed information.

45. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

storing digital signal processor operands in an integrated circuit alterable memory;

generating input information;

generating pattern recognition information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the pattern recognition information.

46. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;

generating pattern recognition information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the pattern recognition information.

48. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

storing digital signal processor operands in an integrated circuit alterable memory;

generating input information;

generating data compressed information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the data compressed information.

49. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;

generating data compressed information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the data compressed information.

57. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

storing digital signal processor operands in an integrated circuit alterable memory;

generating input information;

generating iteratively processed information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the iteratively processed information.

58. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;

generating iteratively processed information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

C4 #1

generating output information in response to the iteratively processed information.

C5 #1

61. (Amended) A comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

storing digital signal processor operands in an integrated circuit alterable memory;

generating input information;

generating searched information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the searched information.

C6 #1

63. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

storing digital signal processor operands in an integrated circuit alterable memory;

generating input information;

generating matched information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the matched information.

C7 #1

70. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;

generating matched information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the matched information.

89. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

storing digital signal processor operands in an integrated circuit alterable memory;

generating input information;

generating transformed information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the transformed information.

90. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;

generating transformed information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the transformed information.

92. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

storing digital signal processor operands in an integrated circuit alterable memory;

generating input information;

generating updated information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the updated information.

94. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;

generating updated information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the updated information.

95. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

storing digital signal processor operands in an integrated circuit alterable memory;

generating input information;

generating correlated information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the correlated information.

96. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;

generating correlated information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the correlated information.

97. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

storing digital signal processor operands in an integrated circuit alterable memory;

generating input information;

generating signature modulated information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the signature modulated information.

100. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;

generating signature modulated information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the signature modulated information.

101. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

storing digital signal processor operands in an integrated circuit alterable memory;

generating input information;

generating RF modulated information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the RF modulated information.

102. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;

generating RF modulated information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the RF modulated information.

105. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

storing digital signal processor operands in an integrated circuit alterable memory;

generating input information;

generating radar image information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the radar image information.

107. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;

generating radar image information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the radar image information.

108. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

storing digital signal processor operands in an integrated circuit alterable memory;

generating input information;

generating medical image information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the medical image information.

110. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;

generating medical image information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the medical image information.

112. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

storing digital signal processor operands in an integrated circuit alterable memory;

generating input information;

generating seismic information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the seismic information.

114. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;

generating seismic information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the seismic information.

116. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

storing digital signal processor operands in an integrated circuit alterable memory;

generating input information;

generating filtered information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the filtered information.

118. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;

generating filtered information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the filtered information.

120. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

generating processed information with an integrated circuit digital signal processor.

122. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

generating processed information with an integrated circuit digital signal processor having an indirect transfer instruction.

124. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

C21 H1

generating input information; and

generating processed information with an integrated circuit digital signal processor having an index instruction.

C22 H1

132. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

generating processed information with an integrated circuit digital signal processor having an interrupt instruction.

C23 H1

140. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

generating processed information with an integrated circuit digital signal processor having a read only memory write instruction.

C24 H1

142. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

generating processed information with an integrated circuit digital signal processor having a decrement instruction.

C25 H1

144. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

C25 H1

generating processed information with an integrated circuit digital signal processor having decrement and transfer instruction.

C26 H1

146. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

generating processed information with an integrated circuit digital signal processor having a conditional transfer instruction.

C27 H1

148. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

generating processed information with an integrated circuit digital signal processor having a looping instruction.

C28 H1

156. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

generating processed information with an integrated circuit digital signal processor having a skip on condition instruction.

157. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

generating processed information with an integrated circuit digital signal processor having a serial input instruction.

158. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

generating processed information with an integrated circuit digital signal processor having a serial output instruction.

159. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

generating processed information with an integrated circuit digital signal processor having discrete output instruction.

166. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

generating processed information with an integrated circuit digital signal processor having a skip on discrete instruction.

168. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

generating processed information with an integrated circuit digital signal processor having a power turn on interrupt instruction.

184. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

generating processed information with an integrated circuit digital signal processor having a save return address microinstruction in response to the digital signal processor program and in response to the input information.

202. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

writing digital signal processor operands into the integrated circuit read only memory in response to the digital signal processor program and in response to the input information.

220. (Amended) A process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;

generating searched information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the searched information.

CLAIMS AS AMENDED WITH UNDERLINES AND BRACKETS

Please amend claims 42, 43, 45, 46, 48, 49, 57, 58, 61, 63, 70, 89, 90, 92, 94 - 97, 100 - 102, 105, 107, 108, 110, 112, 114, 116, 118, 120, 122, 124, 132, 140, 142, 144, 146, 148, 156 - 159, 166, 168, 184, 202, and 220, as follows:

42. (Amended) A [filter processor system as set forth in claim 41, further] process comprising the acts of:

[a sound circuit coupled to the integrated circuit output circuit and generating electrical sound information in response to the digital output information; and

a sound transducer coupled to the sound circuit and generating an acoustic sound in response to the electrical sound information]

storing a digital signal processor program in an integrated circuit read only memory;

storing digital signal processor operands in an integrated circuit alterable memory;

generating input information;

generating signal processed information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the signal processed information.

43. (Amended) A [filter processor system as set forth in claim 41, further] process comprising the acts of:

[a display circuit coupled to the integrated circuit output circuit and generating a display information in response to the digital output information; and

a display monitor coupled to the display circuit and generating a display in response to the display information]

storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;

generating signal processed information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the signal processed information.

45. (Amended) A [filter processor system as set forth in claim 41, wherein the integrated circuit output circuit is an integrated circuit serial output circuit generating the digital output information as serial digital output information in response to the in response to the filter processed information and in response to the computer program] process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

storing digital signal processor operands in an integrated circuit alterable memory;

generating input information;

generating pattern recognition information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the pattern recognition information.

46. (Amended) A [filter processor system as set forth in claim 41, wherein the analog to digital converter generates the digital information as serial digital information and wherein the integrated circuit input circuit is an integrated circuit serial input circuit coupled to the integrated circuit read only memory and to the analog to digital converter and generating the input information in response to the serial digital information and in response to the computer program] process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;

generating pattern recognition information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the pattern recognition information.

48. (Amended) A [receiver system as set forth in claim 47, further] process comprising the acts of:

[a sound circuit coupled to the integrated circuit output circuit and generating electrical sound information in response to the output information and

a sound transducer coupled to the sound circuit and generating an acoustic sound in response to the electrical sound information]

storing a digital signal processor program in an integrated circuit read only memory;

storing digital signal processor operands in an integrated circuit alterable memory;

generating input information;

generating data compressed information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the data compressed information.

49. (Amended) A [receiver system as set forth in claim 47, further] process comprising the acts of:

[a display circuit coupled to the integrated circuit output circuit and generating display information in response to the output information and

a display monitor coupled to the display circuit and generating a display in response to the display information]

storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;

generating data compressed information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the data compressed information.

57. (Amended) A [digital signal processor as set forth in claim 53, wherein the integrated circuit output circuit is an integrated circuit serial output circuit generating the digital output information as serial digital output information in response to the filter processed information and in response to the processing program] process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

storing digital signal processor operands in an integrated circuit alterable memory;

generating input information;

generating iteratively processed information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the iteratively processed information.

58. (Amended) A [digital signal processor as set forth in claim 53, wherein the integrated circuit input circuit is an integrated circuit serial input circuit coupled to the integrated circuit read only memory and generating the input information as serial input information and in response to the processing program] process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;

generating iteratively processed information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the iteratively processed information.

61. (Amended) A [filter processor implemented on a single integrated circuit chip as set forth in claim 59, further] comprising the acts of:

[an integrated circuit synchronization circuit generating synchronization information, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

wherein the integrated circuit processing circuit is coupled to the integrated circuit synchronization circuit and further generates the filtered operands in response to the synchronization information]

storing a digital signal processor program in an integrated circuit read only memory;

storing digital signal processor operands in an integrated circuit alterable memory;

generating input information;

generating searched information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the searched information.

63. (Amended) A [filter processor implemented on a single integrated circuit chip as set forth in claim 59, wherein the integrated circuit processing circuit is an integrated circuit multiple loop iterative processing circuit iteratively generating the filtered operands with multiple iterative loops] process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

storing digital signal processor operands in an integrated circuit alterable memory;

generating input information;

generating matched information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the matched information.

70. (Amended) A [filter processor implemented on a single integrated circuit chip as set forth in claim 65, wherein the integrated circuit alterable memory includes an integrated circuit dynamic random access alterable memory dynamically storing operands, said filter processor further comprising a refresh circuit coupled to the integrated circuit alterable memory and refreshing the integrated circuit alterable memory] process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;

generating matched information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the matched information.

89. (Amended) A [An integrated circuit filter processor system as set forth in claim 87, further] process comprising the acts of:

[an integrated circuit synchronization circuit generating synchronization information;

wherein the integrated circuit processing circuit is coupled to the integrated circuit synchronization circuit and further generates the filtered operands in response to the synchronization information]

storing a digital signal processor program in an integrated circuit read only memory;

storing digital signal processor operands in an integrated circuit alterable memory;

generating input information;

generating transformed information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the transformed information.

90. (Amended) A [An integrated circuit filter processor system as set forth in claim 87, wherein the integrated circuit processing circuit is an integrated circuit iterative processing circuit iteratively generating the filtered operands] process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;

generating transformed information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the transformed information.

92. (Amended) A [An integrated circuit filter processor system as set forth in claim 87, wherein the integrated circuit alterable memory includes an integrated circuit dynamic random access alterable memory dynamically storing operands, said filter processor further] process comprising [a refresh circuit coupled to the integrated circuit alterable memory and refreshing the integrated circuit alterable memory] the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

storing digital signal processor operands in an integrated circuit alterable memory;

generating input information;

generating updated information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the updated information.

94. (Amended) A [An integrated circuit filter processor as set forth in claim 86, further] process comprising the acts of:

[an integrated circuit synchronization circuit generating synchronization information;

wherein the integrated circuit processing circuit is coupled to the integrated circuit synchronization circuit and further generates the filtered operands in response to the synchronization information]

storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;

generating updated information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the updated information.

95. (Amended) A [An integrated circuit filter processor as set forth in claim 86, wherein the integrated circuit processing circuit is an integrated circuit iterative processing circuit iteratively generating the filtered operands] process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

storing digital signal processor operands in an integrated circuit alterable memory;

generating input information;

generating correlated information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the correlated information.

96. (Amended) A [An integrated circuit filter processor as set forth in claim 86, wherein the integrated circuit processing circuit is an integrated circuit multiple loop iterative processing circuit iteratively generating the filtered operands with multiple iterative loops] process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;

generating correlated information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the correlated information.

97. (Amended) A [An integrated circuit filter processor as set forth in claim 86, wherein the integrated circuit alterable memory includes an integrated circuit dynamic random access alterable memory dynamically storing operands, said filter processor further comprising a refresh circuit coupled to the integrated circuit alterable memory and refreshing the integrated circuit alterable memory] process comprising the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

storing digital signal processor operands in an integrated circuit alterable memory;
generating input information;
generating signature modulated information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and
generating output information in response to the signature modulated information.

100. (Amended) A [system comprising the digital signal processor as set forth in claim 98, the system further] process comprising [;
a machine controller coupled to the integrated circuit instruction execution circuit and generating machine control information in response to the processed information generated by the integrated circuit instruction execution circuit; and
a machine coupled to the machine controller and operating in response to the machine control information generated by the machine controller] the acts of:
storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;
storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;
generating input information;
generating signature modulated information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and
generating output information in response to the signature modulated information.

101. (Amended) A [system comprising the digital signal processor as set forth in claim 98, the system further] process comprising [;
a communication circuit coupled to the integrated circuit instruction execution circuit and communicating information to a remote location in response to the processed information generated by the integrated circuit instruction execution circuit] the acts of:
storing a digital signal processor program in an integrated circuit read only memory;
storing digital signal processor operands in an integrated circuit alterable memory;
generating input information;
generating RF modulated information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and
generating output information in response to the RF modulated information.

102. (Amended) A [system comprising the digital signal processor as set forth in claim 98, the system further] process comprising [;
a display circuit coupled to the integrated circuit instruction execution circuit and generating display information in response to the processed information generated by the integrated circuit instruction execution circuit; and
a display device coupled to the display circuit and displaying information in response to the display information generated by the display circuit] the acts of:
storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;
storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;
generating input information;
generating RF modulated information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and
generating output information in response to the RF modulated information.

105. (Amended) A [system comprising the digital signal processor as set forth in claim 104, the system further] process comprising [;
a machine controller coupled to the integrated circuit instruction execution circuit and generating machine control information in response to the first processed information generated by the integrated circuit instruction execution circuit; and
a machine coupled to the machine controller and operating in response to the machine control information generated by the machine controller] the acts of:
storing a digital signal processor program in an integrated circuit read only memory;
storing digital signal processor operands in an integrated circuit alterable memory;
generating input information;
generating radar image information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and
generating output information in response to the radar image information.

107. (Amended) A [system comprising the digital signal processor as set forth in claim 104, the system further] process comprising [;
a display circuit coupled to the integrated circuit instruction execution circuit and generating display information in response to the first processed information generated by the integrated circuit instruction execution circuit; and
a display device coupled to the display circuit and displaying information in response to the display information generated by the display circuit] the acts of:
storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;
storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;
generating radar image information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and
generating output information in response to the radar image information.

108. (Amended) A [system comprising the digital signal processor as set forth in claim 104, the system further] process comprising [;
a graphics circuit coupled to the integrated circuit instruction execution circuit and generating graphics information in response to the first processed information generated by the integrated circuit instruction execution circuit; and
a graphics display device coupled to the graphics circuit and displaying graphics images in response to the graphics information generated by the graphics circuit] the acts of:
storing a digital signal processor program in an integrated circuit read only memory;
storing digital signal processor operands in an integrated circuit alterable memory;
generating input information;
generating medical image information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and
generating output information in response to the medical image information.

110. (Amended) A [system comprising the digital signal processor as set forth in claim 109, the system further] process comprising [;
a communication circuit coupled to the integrated circuit instruction execution circuit and communicating information to a remote location in response to the first processed information generated by the integrated circuit instruction execution circuit] the acts of:
storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;
storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;
generating input information;
generating medical image information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and
generating output information in response to the medical image information.

112. (Amended) A [system comprising the digital signal processor as set forth in claim 111, the system further] process comprising [;
a display circuit coupled to the integrated circuit instruction execution circuit and generating display information in response to the first processed information generated by the integrated circuit instruction execution circuit; and
a display device coupled to the display circuit and displaying information in response to the display information generated by the display circuit] the acts of:
storing a digital signal processor program in an integrated circuit read only memory;
storing digital signal processor operands in an integrated circuit alterable memory;
generating input information;
generating seismic information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and
generating output information in response to the seismic information.

114. (Amended) A [system comprising the digital signal processor as set forth in claim 113, the system further] process comprising [;
a graphics circuit coupled to the integrated circuit instruction execution circuit and generating graphics information in response to the first processed information generated by the integrated circuit instruction execution circuit; and
a graphics display device coupled to the graphics circuit and displaying graphics images in response to the graphics information generated by the graphics circuit] the acts of:
storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;
storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;
generating input information;
generating seismic information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and
generating output information in response to the seismic information.

116. (Amended) A [system comprising the digital signal processor as set forth in claim 115, the system further] process comprising [;
a machine controller coupled to the integrated circuit instruction execution circuit and generating machine control information in response to the first processed information generated by the integrated circuit instruction execution circuit; and
a machine coupled to the machine controller and operating in response to the machine control information generated by the machine controller] the acts of:
storing a digital signal processor program in an integrated circuit read only memory;
storing digital signal processor operands in an integrated circuit alterable memory;
generating input information;
generating filtered information in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the filtered information.

118. (Amended) A [system comprising the digital signal processor as set forth in claim 117, the system further] process comprising [;

a communication circuit coupled to the integrated circuit instruction execution circuit and communicating information to a remote location in response to the first processed information generated by the integrated circuit instruction execution circuit] the acts of:

storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;

generating filtered information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the filtered information.

120. (Amended) A [system comprising the digital signal processor as set forth in claim 119, the system further] process comprising [;

a display circuit coupled to the integrated circuit instruction execution circuit and generating display information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a display device coupled to the display circuit and displaying information in response to the display information generated by the display circuit] the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

generating processed information with an integrated circuit digital signal processor.

122. (Amended) A [system comprising the digital signal processor as set forth in claim 121, the system further] process comprising [;

a graphics circuit coupled to the integrated circuit instruction execution circuit and generating graphics information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a graphics display device coupled to the graphics circuit and displaying graphics images in response to the graphics information generated by the graphics circuit] the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

generating processed information with an integrated circuit digital signal processor having an indirect transfer instruction.

124. (Amended) A [system comprising the digital signal processor as set forth in claim 123, the system further] process comprising [;

a display circuit coupled to the integrated circuit instruction execution circuit and generating display information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a display device coupled to the display circuit and displaying information in response to the display information generated by the display circuit] the acts of:

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

generating processed information with an integrated circuit digital signal processor having an index instruction.

132. (Amended) A [system comprising the integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 131, the system further] process comprising the acts of:

[a machine controller coupled to the integrated circuit instruction execution circuit and generating machine control information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a machine coupled to the machine controller and operating in response to the machine control information generated by the machine controller]

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

generating processed information with an integrated circuit digital signal processor having an interrupt instruction.

140. (Amended) A [system comprising the integrated circuit digital signal processor as set forth in claim 139, the system further] process comprising the acts of:

[a communication circuit coupled to the integrated circuit instruction execution circuit and communicating information to a remote location in response to the first processed information generated by the integrated circuit instruction execution circuit]

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

generating processed information with an integrated circuit digital signal processor having a read only memory write instruction.

142. (Amended) A [system] process comprising [the integrated circuit digital signal processor as set forth in claim 141, the system further comprising] the acts of:

[a display circuit coupled to the integrated circuit instruction execution circuit and generating display information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a display device coupled to the display circuit and displaying information in response to the display information generated by the display circuit]

storing a digital signal processor program in an integrated circuit read only memory;
generating input information; and
generating processed information with an integrated circuit digital signal processor having a decrement instruction.

144. (Amended) A [system comprising the integrated circuit digital signal processor as set forth in claim 143, the system further] process comprising the acts of:
[a graphics circuit coupled to the integrated circuit instruction execution circuit and generating graphics information in response to the first processed information generated by the integrated circuit instruction execution circuit; and
a graphics display device coupled to the graphics circuit and displaying graphics images in response to the graphics information generated by the graphics circuit]
storing a digital signal processor program in an integrated circuit read only memory;
generating input information; and
generating processed information with an integrated circuit digital signal processor having decrement and transfer instruction.

146. (Amended) A [system comprising the integrated circuit digital signal processor as set forth in claim 145, the system further] process comprising the acts of:
[a machine controller coupled to the integrated circuit instruction execution circuit and generating machine control information in response to the first processed information generated by the integrated circuit instruction execution circuit; and
a machine coupled to the machine controller and operating in response to the machine control information generated by the machine controller]
storing a digital signal processor program in an integrated circuit read only memory;
generating input information; and
generating processed information with an integrated circuit digital signal processor having a conditional transfer instruction.

148. (Amended) A [system comprising the integrated circuit digital signal processor as set forth in claim 147, the system further] process comprising the acts of:
[a machine controller coupled to the integrated circuit instruction execution circuit and generating machine control information in response to the first processed information generated by the integrated circuit instruction execution circuit; and
a machine coupled to the machine controller and operating in response to the machine control information generated by the machine controller]
storing a digital signal processor program in an integrated circuit read only memory;
generating input information; and
generating processed information with an integrated circuit digital signal processor having a looping instruction.

156. (Amended) A [system comprising the integrated circuit digital signal processor as set forth in claim 155, the system further] process comprising the acts of:
[a machine controller coupled to the integrated circuit instruction execution circuit and generating machine control information in response to the first processed information generated by the integrated circuit instruction execution circuit; and
a machine coupled to the machine controller and operating in response to the machine control information generated by the machine controller]
storing a digital signal processor program in an integrated circuit read only memory;
generating input information; and
generating processed information with an integrated circuit digital signal processor having a skip on condition instruction.

157. (Amended) A [system comprising the integrated circuit digital signal processor as set forth in claim 155, the system further] process comprising the acts of:
[a communication circuit coupled to the integrated circuit instruction execution circuit and communicating information to a remote location in response to the first processed information generated by the integrated circuit instruction execution circuit]
storing a digital signal processor program in an integrated circuit read only memory;
generating input information; and
generating processed information with an integrated circuit digital signal processor having a serial input instruction.

158. (Amended) A [system comprising the integrated circuit digital signal processor as set forth in claim 155, the system further] process comprising the acts of:
[a display circuit coupled to the integrated circuit instruction execution circuit and generating display information in response to the first processed information generated by the integrated circuit instruction execution circuit; and
a display device coupled to the display circuit and displaying information in response to the display information generated by the display circuit]
storing a digital signal processor program in an integrated circuit read only memory;
generating input information; and
generating processed information with an integrated circuit digital signal processor having a serial output instruction.

159. (Amended) A [system comprising the integrated circuit digital signal processor as set forth in claim 155, the system further] process comprising the acts of:
[a graphics circuit coupled to the integrated circuit instruction execution circuit and generating graphics information in response to the first processed information generated by the integrated circuit instruction execution circuit; and

a graphics display device coupled to the graphics circuit and displaying graphics images in response to the graphics information generated by the graphics circuit]

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

generating processed information with an integrated circuit digital signal processor having discrete output instruction.

166. (Amended) A [digital signal processor system as set forth in claim 165, further] process comprising the acts of:

[a serial display communication channel coupled to the integrated circuit data processor and communicating serial display information in response to the processed information generated by the integrated circuit data processor; and

a display device coupled to the serial display communication channel and displaying machine information in response to the serial display information communicated by the serial display communication channel]

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

generating processed information with an integrated circuit digital signal processor having a skip on discrete instruction.

168. (Amended) A [digital signal processor system as set forth in claim 165, further] process comprising the acts of:

[a serial communication link coupled to the integrated circuit data processor and communicating serial information in response to the processed information generated by the integrated circuit data processor;

a storing circuit coupled to the serial communication link and storing output machine information in response to the serial output information communicated by the serial communication link; and

a machine circuit coupled to the storing circuit and generating machine information in response to the output machine information stored in the storing circuit]

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

generating processed information with an integrated circuit digital signal processor having a power turn on interrupt instruction.

184. (Amended) A process [of operating a system] comprising [the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 178, the process further comprising] the acts of: [making a product in response to the processed information]

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

generating processed information with an integrated circuit digital signal processor having a save return address microinstruction in response to the digital signal processor program and in response to the input information.

202. (Amended) A process [of operating a system comprising the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 200, the process further] comprising the acts of: [making a product in response to the second processed information]

storing a digital signal processor program in an integrated circuit read only memory;

generating input information; and

writing digital signal processor operands into the integrated circuit read only memory in response to the digital signal processor program and in response to the input information.

220. (Amended) A process [of operating a system] comprising [the process of operating an integrated circuit digital signal processor implemented on a single integrated circuit chip as set forth in claim 214, the process further comprising] the acts of: [making an electric product in response to the second processed information]

storing a digital signal processor program in an integrated circuit read only memory, the integrated circuit read only memory implemented on a single integrated circuit chip;

storing digital signal processor operands in an integrated circuit alterable memory, the integrated circuit alterable memory implemented on the single integrated circuit chip;

generating input information;

generating searched information with an integrated circuit digital signal processor in response to the digital signal processor program, in response to the digital signal processor operands, and in response to the input information; and

generating output information in response to the searched information.